Gwani Software

Training Department

(Knowledge & Expertise)

Computer_Architecture_&_Organisation Curriculum

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Warning

Proposed by

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Approved for usage by

Al-Ameen Abubakar, Director Training, this 5th day of Muharram, 1433 equivalent to

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Gwani Software

TRAINING DEPARTMENT

Computer Architecture & Organization

Description: - This course is intended to give the trainee the basic knowledge of how computer system is internally built up. The build up is restricted to hardware components.

Aims: - The aims of this course are:

1. To avail the trainee with the knowledge of how computer hardware are internally manufactured.
2. To drill the trainee with the basic calculations regarding the internal components of a computer system.
3. To avail the trainee with the knowledge of how computer hardware functions.
4. To introduce to the trainee, the elementary knowledge of mathematics and electronic that are fundamentals to the Internal design of hardware.
5. To inspect common architecture of hardware design.

Objectives: - The trainee at the end of the training session should be able to;

- Know how computer hardware are internally manufactured by OEM.
- Understand the basic calculations regarding the internal components of a computer system.
- Understand how several hardware functions inside computer system.

- Understand the elementary mathematical and electronics theories that form the foundation of computer architecture and organization.
- Understand the common architecture used in the hardware manufacturing companies.
- Understand reasons behind common architectures used in the hardware manufacturing companies.

Target Audience: - This course should be taken by computer architects, hardware Engineers, hardware Technicians, Staff of hardware manufacturing companies, hardware vendors, and electronics engineers.

Pre-requisite: - pre-requisite course include assembly language, system software care, and PC Maintenance. Knowledge of design of electronics is an added advantage.

Approximate Duration: - This course requires 30 hours of class sessions.

Method of Assessment: - Trainees are to be assessed with an examination on lessons covered.

Methodology: - The class takes a lesson discusses it, elaborating on practical examples regarding the lesson. The training will equally be shown the basic laws of mathematics and physics surrounding the (hardware) lessons discussed.

Recommended Resource Materials: - the following materials are recommended for the trainee study;

1. Linda Null & Julia Lobur, (2003) “The Essentials of Computer Organization and Architecture”, Jones and Barleff publishers, Massachusetts.

Day	Lesson
1.	**Introduction: -**the main components of a computer, tear down of computer system, standard organizations, historical development; first generation, second generation, third generation, fourth generation, fifth generation, computer level hierarchy, von Neumann models, Non von Neumann models.
2.	**Data representation in Computer systems: -** positional number systems, decimal to binary conversion: unsigned whole numbers, converter fractions, converter, between power-of-two radices.
3.	**Data representation continued: -** Signed Integer representation: - signed magnitude, complement systems. Floating point representation: a simple model, floating point arithmetic, floating point errors, IEEE-754 floating point standard.
4.	**Data representation continued: -** character codes; -BCD, EBCDIC, ASCII & Unicode.
5.	**Boolean Algebra & Digital logic: -** Boolean algebra; Boolean expressions, complements, representing simplification of Boolean expressions, complements, representing Boolean functions. Logic gates: symbols for logic continued.
6.	**Boolean Algebra & Digital logic continued: -** Digital components: - Digital circuits & their relationship to Boolean Algebra, Integrated circuits. Combinational circuits: - basic concepts, examples of typical combinational circuits, sequential circuits: - basic concepts, clocks, flip flops, examples of

	sequential circuits. **Karnaugh maps: -** Description of K maps & terminology, K map simplification for 2 variables, 3 variables and 4 variables. Don't care conditions.
7.	**An Introduction to a simple Computer (MARIE), Introduction: -** CPU basics & organization, the bus, clocks, the input/output subsystem, memory organization & addressing interrupts.
8.	**Memory: -** Types of memory, memory hierarchy, cache memory. Cache memory: cache mapping schemes, replacement policies effective access time & hit radio, cache write policies.
9.	**Memory continued: -** virtual memory: paging, effective access time using paging, putting it all together, using cache, TLBS & paging, advantages and disadvantages of paging & virtual memory, segmentation, paging combined with segmentation.
10.	**Input/Output storage systems:** Introduction, Amdahl's law. 1/0 Architectures: - 1/0 control methods, 1/0 bus operation, interrupt- driven 1/o.
11.	**Input/ Output storage systems continued: -** magnetic disk Technology: rigid disk drives, flexible (floppy) disks. Optical disks: - CD-ROM, DVD, Optical Disk recording Methods.
12.	**Input/Output storage systems continued: -** Magnetic tape. RAID: - RAID level 0, RAID level 1, RAID level 2, RAID level 3, RAID level 4, RAID level %, RAID level 6, Hybrid RAID systems.
13.	**Input/Output storage systems continued: -** Data compression: - statistical coding, 2iv- Lempel (1-2) Dictionary systems, GIF compression, JPEG compression,

14.	**System Software: -** o/s history, o/s design, o/s services. Protected Environments: - Virtual machines, subsystems and partitions, protected environments & Evolution of systems Architectures.
15.	**System Software continued: -** programming tools: - Assemblers & assembly, link editors, dynamic link libraries, compilers, Interpreters. Java translator, database Software, transaction managers.
16.	**Alternative Architectures: -** Introduction, RISC Machines, Flynn's Taxonomy parallel & multi processor Architectures.
17.	**Alternative Architecture continued: -** parallel & multi processor Architectures; - superscalar & VLLIW Vector processors, Interconnection Networks, shared memory multiprocessors, Distributed circuitry.
18.	**Alternative Architecture continued: -** Alternative parallel processor approaches: - Data flow circuitry Neural networks, systolic arrays.
19.	**Performance Measurement & Analysis: -** Introduction, basic computer performance equation, mathematical preliminaries.
20.	**Performance Measurement & Analysis continued: -** Bench marking; clock rate, MIPS, Flops, systems simulation.
21.	**Performance Measurement & Analysis continued: -** CPU performance optimization: - branch optimization, algorithms & simple code.
22.	**Performance Measurement & Analysis continued: -** Disk performance: - understanding the problem, physical consideration, logical considerations.
23.	**Network Organization & Architecture: -** Introduction**,** early business computer networks, early academic & scientific networks; the roots & Architecture of the Internet. Network protocols I: - ISO/OSI protocol; - a parable, OSI reference model.
24.	**Network Organization & Architecture continued: -** Network protocols II;

	TCP/IP Network Architecture: - I player for version 4, trouble with version 4, transmission control protocol, TCP protocol, IP version 6.
25.	**Network Organization & Architecture continued: -** Network organization: - physical transmission media Interface cards, repeaters, hubs, switches, bridges and gateways, routers and routing.
26.	**Network Organization & Architecture continued: -** High- capacity, digital links; - Digital hierarchy, ISDN, Asynchronous transfer mode. Internet: - ramping on to the internet, ramping up the Internet.
27.	**Introduction to Assembly language code Instruction formats; -** design decision internal storage in the CPU, stacks, registers, operands. Addressing: - Data types, address modes.
28.	**Introduction to Assembly & Architecture continued: -** sample programs using a simulator.
29.	**Review of all assignments & Assessments**
30.	**Revision.**